19-2418; Rev 0; 4/02

MAXIM

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

General Description

The DG411F/DG412F/DG413F are quad, single-pole/single-throw (SPST), fault-protected analog switches. They are pin compatible with the industry-standard nonprotected DG411/DG412/DG413. These new switches feature fault-protected inputs and Rail-to-Rail® signal-handling capability. All terminals are protected from overvoltage faults up to ±36V with power on and up to ±40V with power off. During a fault condition, the COM, NO, or NC terminal becomes an open circuit and only microamperes of leakage current flow from the source. On-resistance is 35Ω (max) and is matched between switches to 1.5Ω (max) at +25°C.

The DG411F has four normally closed (NC) switches. The DG412F has four normally open (NO) switches. The DG413F has two NC and two NO switches. These CMOS switches operate with dual power supplies ranging from ±4.5V to ±20V or a single supply between +9V and +36V. All digital inputs have +0.8V and +2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility when using ±15V or a single +12V supply.

For supply voltages of ±5V, +5V, and +3V, refer to the MAX4711/MAX4712/MAX4713 data sheet.

Applications

Communication Systems

Signal Routing

Test Equipment

Data Acquisition

Industrial and Process Control Systems

Avionics

Redundant/Backup Systems

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Functional Diagram appears at end of data sheet.

Pin Configurations continued at end of data sheet.

Features

- **No Power-Supply Sequencing Required**
- **Rail-to-Rail Signal Handling**
- **All Switches Off with Power Off**
- **All Switches Off when V+ is Off and V- is On**
- **±40V Fault Protection with Power Off**
- **±36V Fault Protection with ±15V Supplies**
- **Control Line Fault Protection from V- - 0.3V to V- + 40V**
- **Pin Compatible with Industry-Standard DG411/DG412/DG413**
- **20ns (typ) Fault Response Time**
- **35Ω (max) R_{ON} with ±15V Supplies**
- **±4.5V to ±20V Dual Supplies**
- **+9V to +36V Single Supply**
- **TTL- and CMOS-Compatible Logic Inputs with ±15V or Single +9V to +15V Supplies**

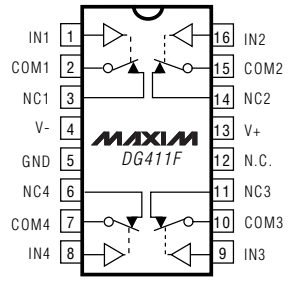
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG411FEUE	-40°C to +85°C	16 TSSOP
DG411FDY	-40°C to +85°C	16 SO
DG411FDJ	-40°C to +85°C	16 Plastic DIP

Ordering Information continued at end of data sheet.

Pin Configurations

TOP VIEW



DIP/TSSOP/SO

DG411F	
LOGIC	**SWITCH**
0	ON
1	OFF

N.C. = NOT CONNECTED. SWITCHES SHOWN FOR LOGIC 0 INPUT.
ALL SWITCHES ARE OFF WITH POWER REMOVED.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V to +44V
V- .....-44V to +0.3V
V+ to V-.....-0.3V to +44V
IN_ ..... (V- - 0.3V) to (V- + 40V)
NO_, NC_ to COM_ (Note1) ..... -40V to +40V
COM_, NO_, NC_ Voltage with
Power On (Note 1)..... -36V to +36V
COM_, NO_, NC_ Voltage with
Power Off (Note 1)..... -40V to +40V
Continuous Current (any terminal) ..... ±30mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle) .....±100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
16-Pin SO (derate 8.7mW/°C above +70°C).....696mW
16-Pin Plastic DIP (derate 10.53mW/°C
above +70°C) 842mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: COM_, NO_, and NC_ pins are fault protected. Signals on COM_, NO_, and NC_ exceeding -36V to +36V may damage the device during power-on conditions. When the power is off, the maximum range is -40V to +40V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±15V Dual Supplies

(V+ = +15V, V- = -15V, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Fault-Free Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$		E	V-		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 10mA, $V_{NO_}$, $V_{NC_}$ = ±10V	+25°C		25	35	Ω
			E			45	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM_}$ = 10mA, $V_{NO_}$, $V_{NC_}$ = ±10V	+25°C		0.2	1.5	Ω
			E			2.0	
On-Resistance Flatness	$R_{FLAT(ON)}$	$I_{COM_}$ = 10mA, $V_{NO_}$, $V_{NC_}$ = ±5V, 0	+25°C		1.0	3	Ω
			E			4	
NO_, NC_ Off-Leakage Current (Note 5)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	$V_{COM_}$ = ±10V, $V_{NO_}$, $V_{NC_}$ = › 10V	+25°C	-0.25	+0.025	+0.25	nA
			E	-20		+20	
COM_ Off-Leakage Current (Note 5)	$I_{COM_(OFF)}$	$V_{COM_}$ = ±10V, $V_{NO_}$, $V_{NC_}$ = › 10V	+25°C	-0.25	+0.025	+0.25	nA
			E	-20		+20	
COM_ On-Leakage Current (Note 5)	$I_{COM_(ON)}$	$V_{COM_}$ = ±10V, $V_{NO_}$, $V_{NC_}$ = ±10V or floating	+25°C	-0.5	+0.025	+0.5	nA
			E	-40		+40	
FAULT							
Fault-Protected Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	V+ = +15V, V- = -15V	E	-36		+36	V
		V+ = 0, V- = -15V	E	-36		+36	
		V+ = V- = 0	E	-40		+40	
NO_ or NC_ Off-Leakage Current	$I_{NO_}$, $I_{NC_}$	$V_{NO_}$, $V_{NC_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	
COM_ Off-Leakage Current	$I_{COM_}$	$V_{COM_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	

ELECTRICAL CHARACTERISTICS—±15V Dual Supplies (continued)

(V+ = +15V, V- = -15V, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
NO_ or NC_ Leakage Current	$I_{NO_}$, $I_{NC_}$	$V_{NO_}$, $V_{NC_}$ = ±40V, V+ = V- = 0	+25°C	-1		+1	µA
			E	-10		+10	
COM_ Leakage Current	$I_{COM_}$	$V_{COM_}$ = ±40V, V+ = V- = 0	+25°C	-1		+1	µA
			E	-10		+10	
NO_ or NC_ Off-Leakage Current	$I_{NO_}$, $I_{NC_}$	V+ = 0, V- = -15V, $V_{NO_}$, $V_{NC_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	
COM_ Off-Leakage Current	$I_{COM_}$	V+ = 0, V- = -15V, $V_{COM_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	
Fault-Trip Threshold			E	V- - 0.4		V+ + 0.4	V
± Fault Output Turn-Off Delay		$V_{NO_}$, $V_{NC_}$ = ±36V, R_L = 1kΩ	E		20		ns
± Fault Recovery Time		$V_{NO_}$, $V_{NC_}$ = ±36V, R_L = 1kΩ	E		1		µs
SWITCH DYNAMICS							
Turn-On Time	t_{ON}	$V_{NO_}$ or $V_{NC_}$ = ±10V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		70	175	ns
			E			220	
Turn-Off Time	t_{OFF}	$V_{NO_}$ or $V_{NC_}$ = ±10V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		55	145	ns
			E			160	
Break-Before-Make Time Delay (DG413F only) (Note 6)	t_{BBM}	$V_{NO_}$ or $V_{NC_}$ = ±10V, R_L = 100Ω, C_L = 10pF, Figure 3	+25°C	2	15		ns
			E	1			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF, Figure 4	+25°C		5		pC
NO_ or NC_ Off-Capacitance	$C_{N_(OFF)}$	f = 1MHz, Figure 5	+25°C		15		pF
COM_ Off-Capacitance	$C_{COM_(OFF)}$	f = 1MHz, Figure 5	+25°C		15		pF
COM_ On-Capacitance	$C_{COM_(ON)}$	f = 1MHz, Figure 5	+25°C		47		pF
Off-Isolation (Note 7)	V_{ISO}	f = 1MHz, R_L = 50Ω, C_L = 15pF, P_{IN} = 0dBm, Figure 6	+25°C		-65		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	f = 1MHz, R_L = 50Ω, C_L = 15pF, P_{IN} = 0dBm, Figure 6	+25°C		-105		dB
LOGIC INPUT							
Input Logic High	V_{IH}		E	2.4			V
Input Logic Low	V_{IL}		E			0.8	V
Input Leakage Current	I_{IN}	$V_{IN_}$ = 0 or V+	E	-1		+1	µA
POWER SUPPLY							
Power-Supply Range	V+, V-		E	±4.5		±20	V
V+ Supply Current	I+	All $V_{IN_}$ = +5V, $V_{COM_}$ = 0	+25°C		355	600	µA
			E			800	
		All $V_{IN_}$ = 0 or V+, $V_{COM_}$ = 0	+25°C		155	300	
			E			400	

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—±15V Dual Supplies (continued)

(V+ = +15V, V- = -15V, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
V- Supply Current	I-	All $V_{IN_}$ = +5V, $V_{COM_}$ = 0	+25°C		155	250	µA
			E			325	
		All $V_{IN_}$ = 0 or V+, $V_{COM_}$ = 0	+25°C		155	250	
			E			325	
GND Supply Current	I_{GND}	All $V_{IN_}$ = +5V, $V_{COM_}$ = 0	+25°C		200	350	µA
			E			475	
		All $V_{IN_}$ = 0 or V+, $V_{COM_}$ = 0	+25°C		0.1	1	
			E			10	

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +12V, V- = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Fault-Free Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$		E	0		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$, $V_{NC_}$ = +10V	+25°C		56	85	Ω
			E			120	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM_}$ = 1mA, $V_{NO_}$, $V_{NC_}$ = +10V	+25°C		1.0	4	Ω
			E			5	
NO_, NC_ Off-Leakage Current (Note 5)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	$V_{COM_}$ = +1V, +10V, $V_{NO_}$, $V_{NC_}$ = +10V, +1V	+25°C	-0.25		+0.25	nA
			E	-20		+20	
COM_ Off-Leakage Current (Note 5)	$I_{COM_(OFF)}$	$V_{COM_}$ = +1V, +10V, $V_{NO_}$, $V_{NC_}$ = +10V, +1V	+25°C	-0.5		+0.25	nA
			E	-20		+20	
COM_ On-Leakage Current (Note 5)	$I_{COM_(ON)}$	$V_{COM_}$ = +1V, +10V, $V_{NO_}$, $V_{NC_}$ = +1V, +10V, or floating	+25°C	-0.5		+0.5	nA
			E	-40		+40	
FAULT							
Fault-Protected Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	Power on	E	-36		+36	V
		Power off	E	-40		+40	
NO_ or NC_ Off-Leakage Current (Note 5)	$I_{NO_}$, $I_{NC_}$	$V_{NO_}$, $V_{NC_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	
COM_ Off-Leakage Current (Note 5)	$I_{COM_}$	$V_{NO_}$, $V_{NC_}$ = ±36V	+25°C	-1		+1	µA
			E	-10		+10	
NO_ or NC_ Leakage Current (Note 5)	$I_{NO_}$, $I_{NC_}$	Supplies off, $V_{NO_}$, $V_{NC_}$ = ±40V	+25°C	-1		+1	µA
			E	-10		+10	

ELECTRICAL CHARACTERISTICS—Single +12V Supply (continued)

(V+ = +12V, V- = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
COM_ Leakage Current (Note 5)	$I_{COM_}$	Supplies off, $V_{NO_}$, $V_{NC_}$ = ±40V	+25°C	-1		+1	µA
			E	-10		+10	
+Fault Output Turn-Off Delay		$V_{NO_}$, $V_{NC_}$ = +36V, R_L = 1kΩ	E		20		ns
+Fault Recovery Time		$V_{NO_}$, $V_{NC_}$ = +36V, R_L = 1kΩ	E		1		µs
SWITCH DYNAMICS							
Turn-On Time	t_{ON}	$V_{NO_}$ or $V_{NC_}$ = +10V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		120	250	ns
			E			315	
Turn-Off Time	t_{OFF}	$V_{NO_}$ or $V_{NC_}$ = +10V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		70	125	ns
			E			140	
Break-Before-Make Time Delay (DG413F Only) (Note 6)	t_{BBM}	$V_{NO_}$ or $V_{NC_}$ = +10V, R_L = 100Ω, C_L = 10pF, Figure 3	+25°C	2	50		ns
			E	1			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF, Figure 4	+25°C		5		pC
LOGIC INPUT							
Input Logic High	V_{IH}		E	2.4			V
Input Logic Low	V_{IL}		E			0.8	V
Input Leakage Current (Note 5)	I_{IN}	$V_{IN_}$ = 0 or V+	E	-1		+1	µA
POWER SUPPLY							
Power-Supply Range	V+		E	+9		+36	V
V+ Supply Current	I+	All $V_{IN_}$ = +5V, $V_{COM_}$ = +6V	+25°C		180	350	µA
			E			450	
		All $V_{IN_}$ = 0 or V+, $V_{COM_}$ = +6V	+25°C		85	150	
			E			250	

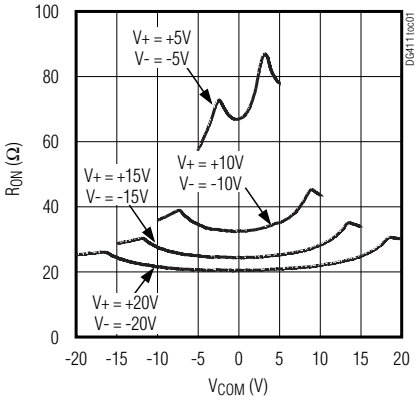
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Electrical specifications at -40°C are not production tested and guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Leakage parameters are 100% tested at maximum rated temperature and with dual supplies and guaranteed by design at +25°C.
Note 6: Guaranteed by design.
Note 7: Off-Isolation = 20 $\log_{10}$ [V_{COM}/(V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

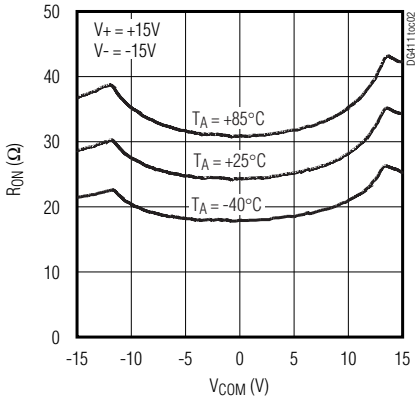
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

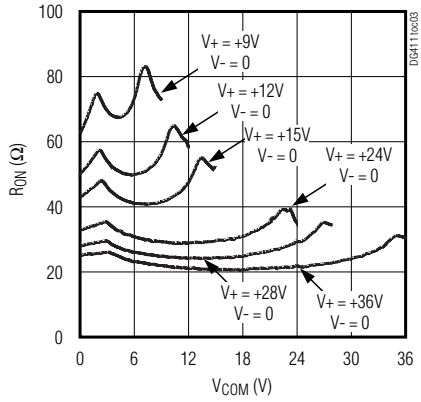
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



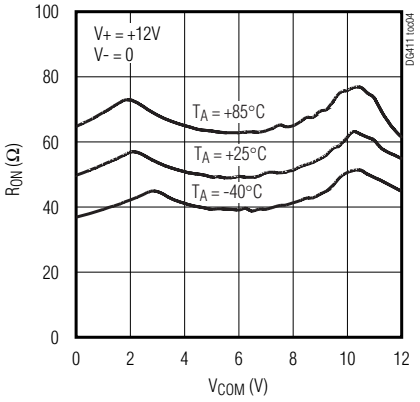
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



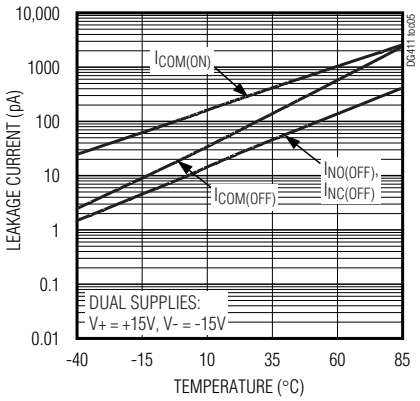
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



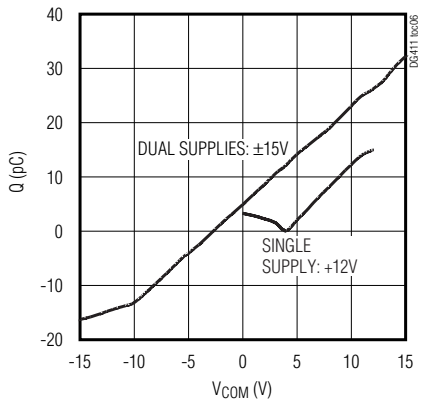
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



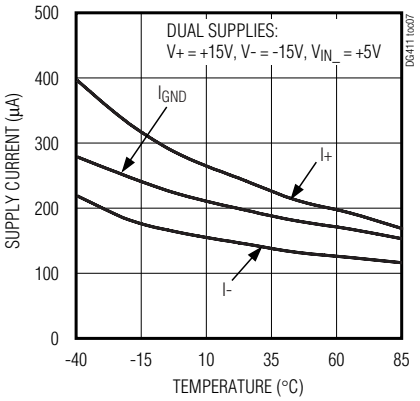
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



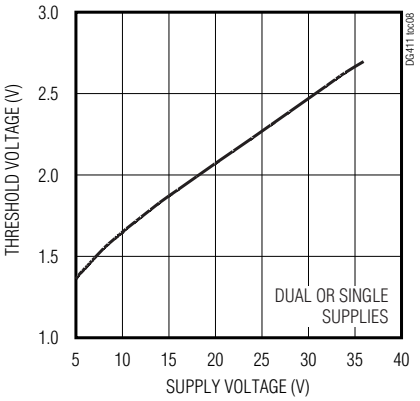
CHARGE INJECTION vs. V_{COM}



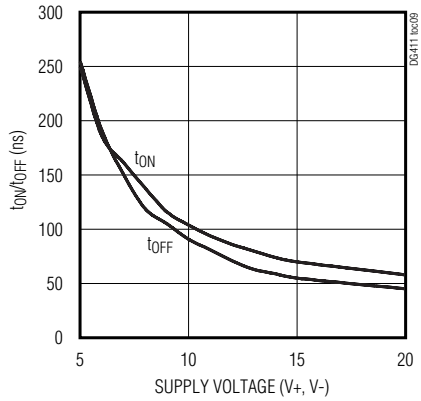
SUPPLY CURRENT vs. TEMPERATURE



LOGIC-LEVEL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



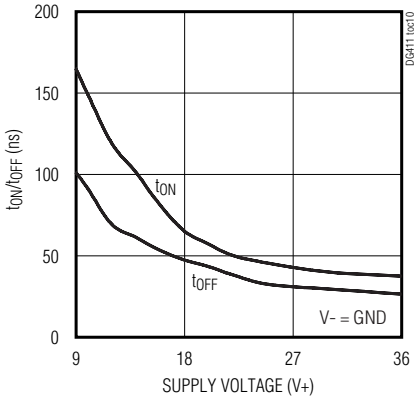
TURN-ON/TURN-OFF TIMES vs. SUPPLY VOLTAGE (DUAL SUPPLIES)



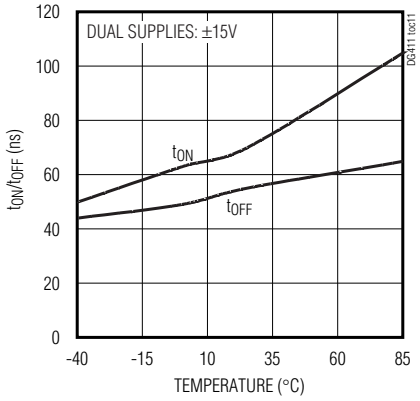
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

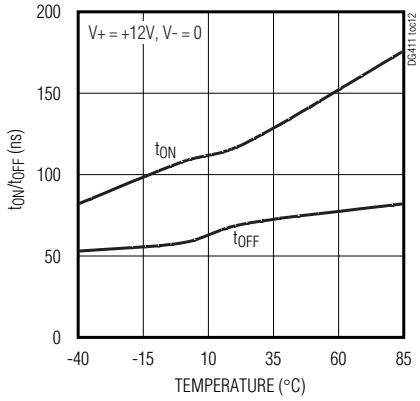
TURN-ON/TURN-OFF TIMES vs. SUPPLY VOLTAGE (SINGLE SUPPLY)



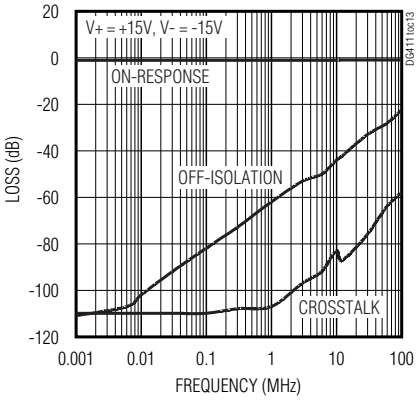
TURN-ON/TURN-OFF TIMES vs. TEMPERATURE (DUAL SUPPLIES)



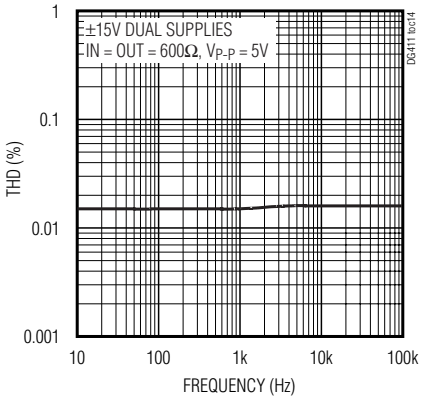
TURN-ON/TURN-OFF TIMES vs. TEMPERATURE (SINGLE SUPPLY)



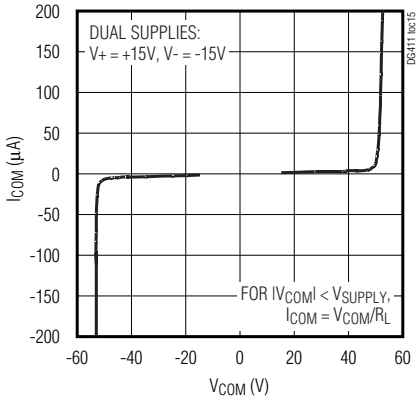
FREQUENCY RESPONSE



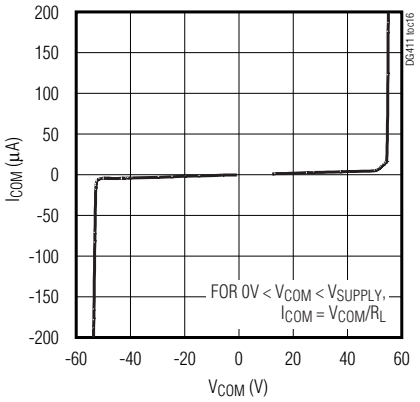
TOTAL HARMONIC DISTORTION vs. FREQUENCY



FAULT CURRENT vs. FAULT VOLTAGE (DUAL SUPPLIES)



FAULT CURRENT vs. FAULT VOLTAGE (SINGLE SUPPLY)

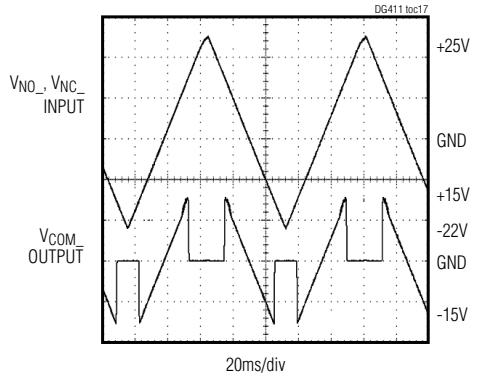


Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

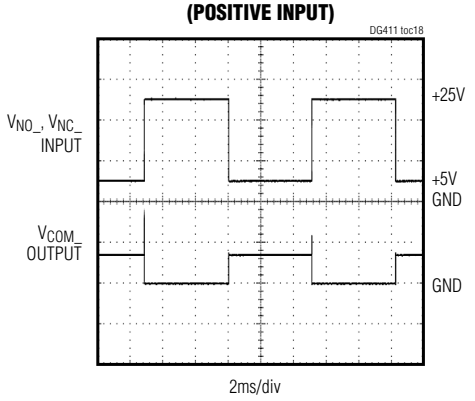
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

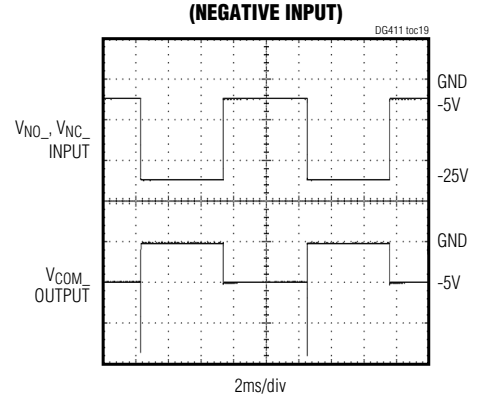
INPUT OVERVOLTAGE vs. OUTPUT



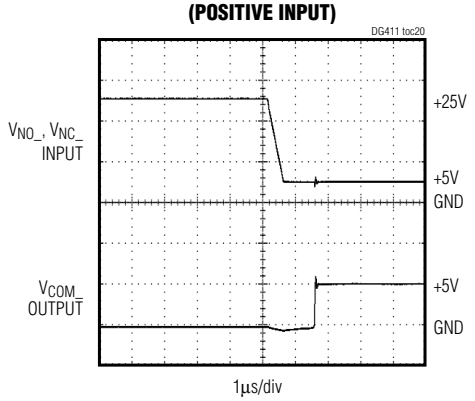
FAULT STEP RESPONSE (POSITIVE INPUT)



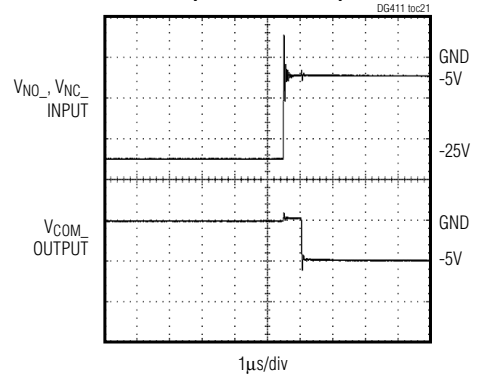
FAULT STEP RESPONSE (NEGATIVE INPUT)



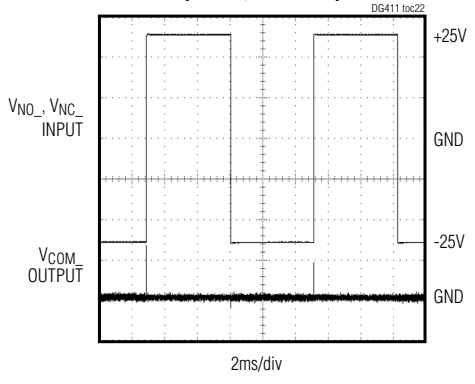
FAULT RECOVERY TIME (POSITIVE INPUT)



FAULT RECOVERY TIME (NEGATIVE INPUT)



FAULT RESPONSE (V+ = 0, V- = -15V)



Pin Description

PIN			NAME	FUNCTION
DG411F	DG412F	DG413F		
1, 16, 9, 8	1, 16, 9, 8	1, 16, 9, 8	IN1, IN2, IN3, IN4	Logic Control Digital Inputs
2, 15, 10, 7	2, 15, 10, 7	2, 15, 10, 7	COM1, COM2, COM3, COM4	Analog Switch Common Terminals
3, 14, 11, 6	—	—	NC1, NC2, NC3, NC4	Analog Switch Normally Closed Terminals
—	3, 14, 11, 6	—	NO1, NO2, NO3, NO4	Analog Switch Normally Open Terminals
—	—	3, 6	NO1, NO4	Analog Switch Normally Open Terminals
—	—	14, 11	NC2, NC3	Analog Switch Normally Closed Terminals
4	4	4	V-	Negative-Supply Voltage Input. Connect to GND for single-supply operation. Bypass with a 0.1µF capacitor to GND.
5	5	5	GND	Ground. Connect to digital ground.
12	12	12	N.C.	No Connection. Not internally connected.
13	13	13	V+	Positive-Supply Voltage Input. Bypass with a 0.1µF capacitor to GND.

Detailed Description

The DG411F/DG412F/DG413F are fault-protected CMOS analog switches with unique operation and construction. These switches differ considerably from traditional fault-protection switches, with several advantages. First, they are constructed with two parallel FETs, allowing very low on-resistance when the switch is on. Second, they allow signals on the NO_ or NC_ pins that are within, or slightly beyond, the supply rails to be passed through the switch to the COM_ terminal (or vice versa), allowing true rail-to-rail signal operation. Third, the DG411F/DG412F/DG413F have the same fault-protection performance on any of the NO_, NC_, or COM_ switch inputs. Operation is identical for both fault polarities. The fault protection extends to ±36V from GND with ±15V supplies.

During a fault condition, the particular overvoltage input (COM_, NO_, NC_) pin becomes high impedance regardless of the switch state or load resistance. When power is removed, the fault protection is still in effect. In this case, the COM_, NO_, or NC_ terminals are a virtual open circuit. The fault can be up to ±40V with power off. The switches turn off when V+ is not powered, regardless of V-.

Pin Compatibility

These switches have identical pinouts to common non-fault-protected CMOS switches. They allow for carefree direct replacement in existing printed circuit boards since the NO_, NC_, and COM_ pins of each switch are fault protected.

Internal Construction

Internal construction is shown in Figure 1, with the analog signal paths shown in bold. A single NO switch is shown. The NC configuration is identical except the logic-level translator becomes an inverter. The analog switch is formed by the parallel combination of N-channel FET (N1) and P-channel FET (P1), which are driven on and off simultaneously according to the input fault condition and the logic-level state.

Normal Operation

Two comparators continuously compare the voltage on the COM_, NO_, and NC_ pins with V+ and V-. When the signal on COM_, NO_, or NC_ is between V+ and V-, the switch acts normally, with FETs N1 and P1 turning on and off in response to IN_ signals. The parallel combination of N1 and P1 forms a low-value resistor between NO_ (or NC_) and COM_ so that signals pass equally well in either direction.

Positive Fault Condition

When the signal on NO_ (or NC_) and COM_ exceeds V+ by about 50mV, the high-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) and COM_ pins high impedance regardless of

the switch state. If the switch state is off, all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance.

Negative Fault Condition

When the signal on NO_ (or NC_) and COM_ exceeds V- by about 50mV, the low-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) and COM_ pins high impedance regardless of the switch state. If the switch state is off, all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance.

Transient Fault Response and Recovery

When a fast rise-time and fall-time transient on NO_, NC_, or COM_ exceeds V+ or V-, the output follows the input to the supply rail with only a few nanoseconds delay. This delay is due to the switch on-resistance and circuit capacitance to ground. When the input transient returns to within the supply rails, however, there is a longer output recovery time delay. For positive faults, the recovery time is typically 1µs. For negative faults, the recovery time is typically 0.5µs. These values depend on the output resistance and capacitance, and are not production tested or guaranteed. The delays are not dependent on the fault amplitude. Higher load resistance and capacitance increase recovery times.

Fault-Protection Voltage and Power Off

The maximum fault voltage on the NO_ (or NC_) and COM_ pins is ±36V with power applied and ±40V with power off.

Failure Modes

Exceeding the fault-protection voltage limits on NO_, NC_, or COM_, even for very short periods, can cause the device to fail. See the *Absolute Maximum Ratings*. The failure modes may not be obvious, and failure in one switch may or may not affect other switches in the same package.

Ground

There is no galvanic connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators. However, the potential of the analog signals must be defined or at least limited with respect to GND.

V+ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the power supplies and the analog signals.

IN_ Logic-Level Thresholds

The logic-level thresholds are CMOS and TTL compatible when V+ is +15V. As V+ is raised, the threshold increases slightly, and when V+ reaches 25V, the level threshold is about 2.3V, above the TTL output high-level minimum of 2.4V, but still compatible with CMOS outputs (see the *Typical Operating Characteristics*). V- has no effect on the logic-level thresholds.

Bipolar Supplies

The DG411F/DG412F/DG413F operate with bipolar supplies between ±4.5V and ±20V. The V+ and V- supplies need not be symmetrical, but their difference cannot exceed the absolute maximum rating of 44V.

Single Supply

The DG411F/DG412F/DG413F operate from a single supply between +9V and +36V when V- is connected to GND.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG412FEUE	-40°C to +85°C	16 TSSOP
DG412FDY	-40°C to +85°C	16 SO
DG412FDJ	-40°C to +85°C	16 Plastic DIP
DG413FEUE	-40°C to +85°C	16 TSSOP
DG413FDY	-40°C to +85°C	16 SO
DG413FDJ	-40°C to +85°C	16 Plastic DIP

Chip Information

TRANSISTOR COUNT: 251

PROCESS: CMOS

SUBSTRATE CONNECTED TO: V+

Test Circuits/Timing Diagrams

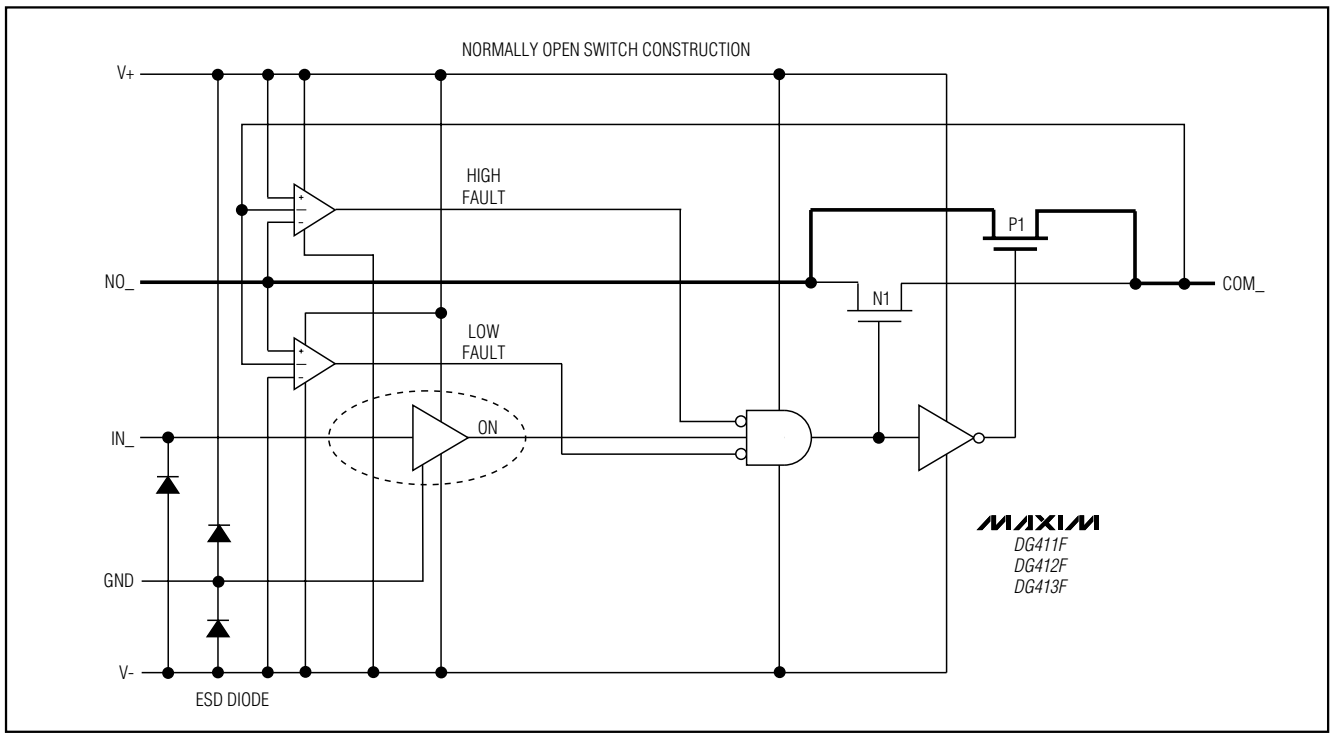


Figure 1. Functional Diagram

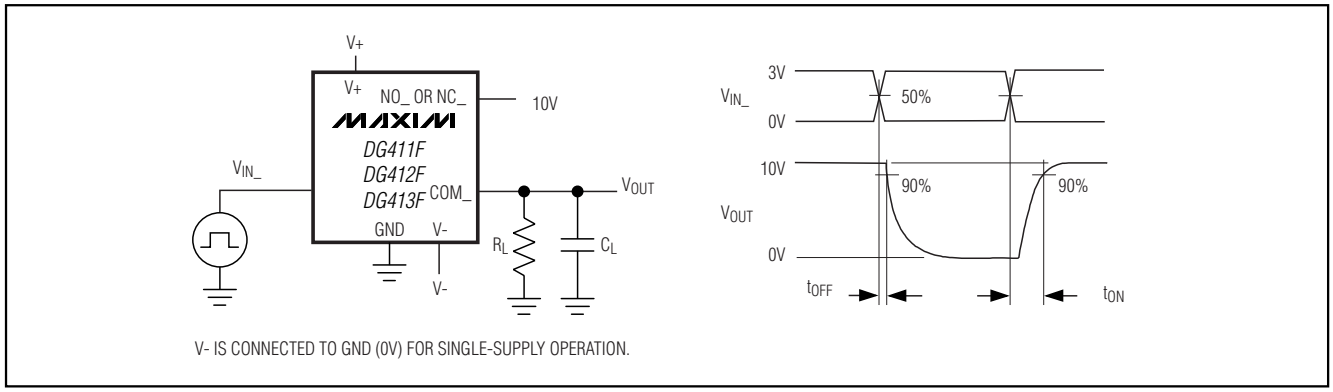


Figure 2. Switch Turn-On/Turn-Off Times

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

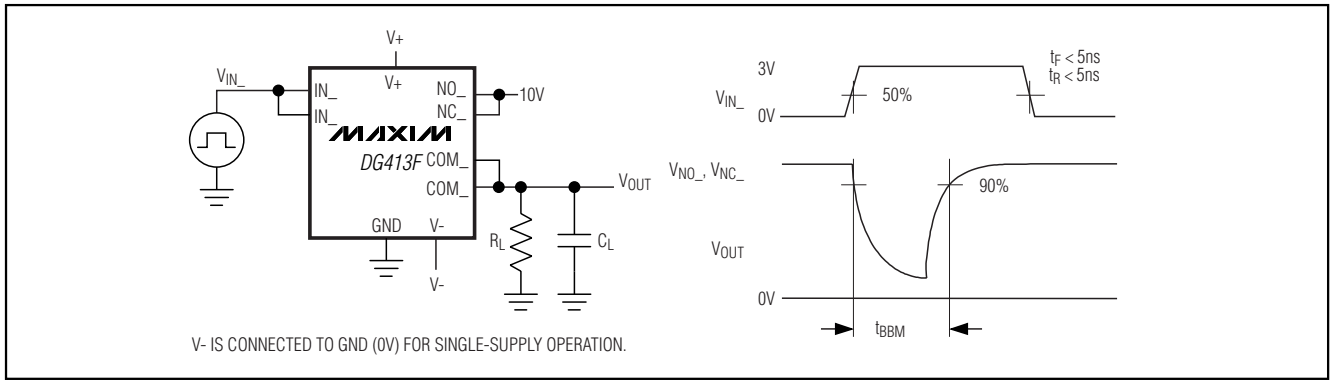


Figure 3. DG413F Break-Before-Make Interval

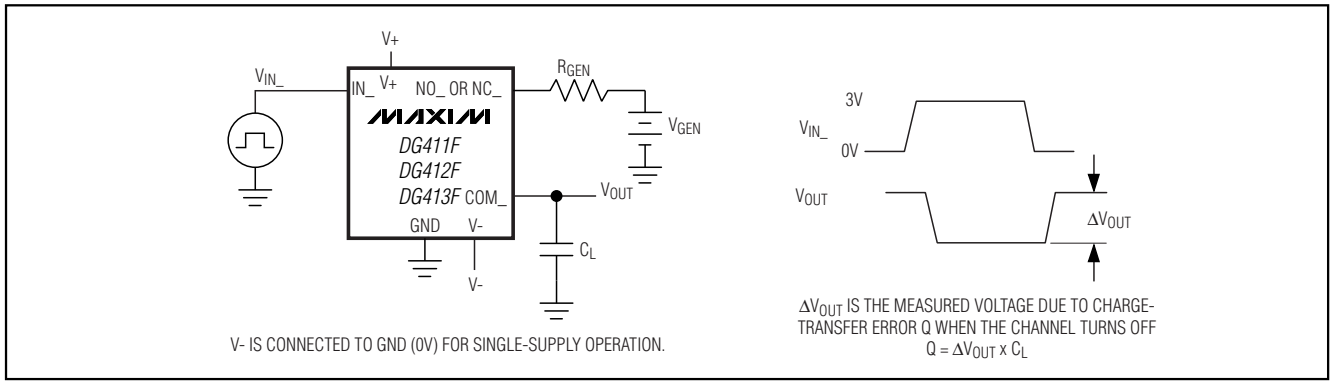


Figure 4. Charge Injection

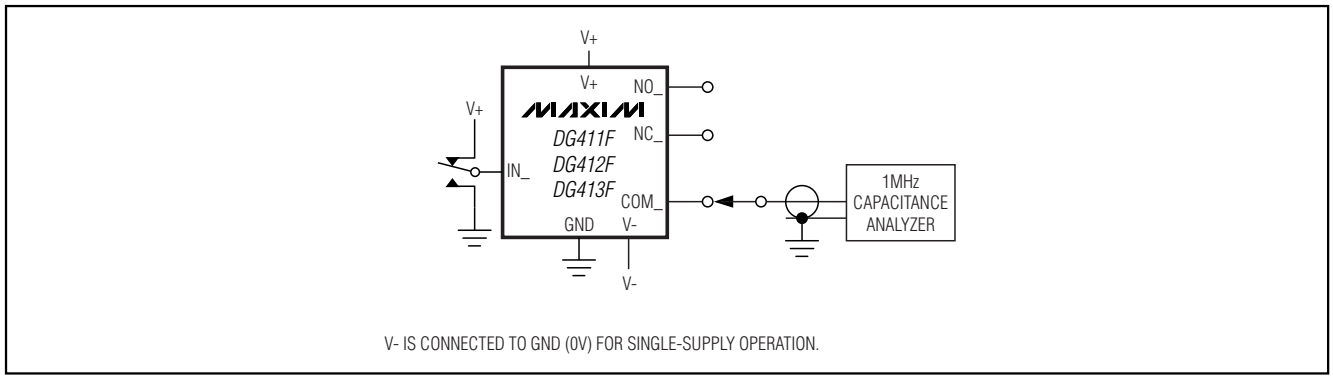
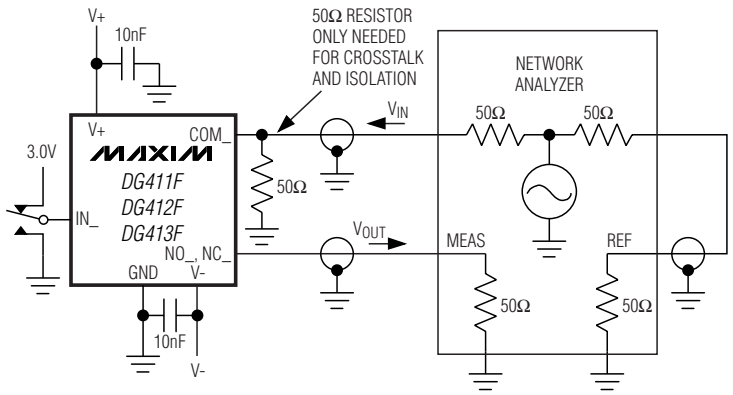


Figure 5. COM_, NO_, NC_ Capacitance

Test Circuits/Timing Diagrams (continued)

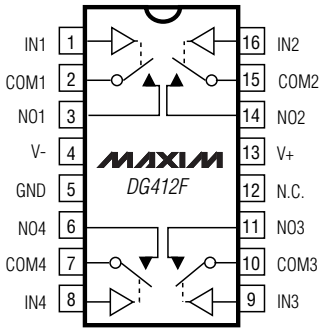


MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AND OPEN AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM_ AND "OFF" NO_ OR NC_ TERMINALS.
ON-RESPONSE IS MEASURED BETWEEN COM_ AND "ON" NO_ OR NC_ TERMINALS.
CROSSTALK IS MEASURED BETWEEN COM_ TERMINALS WITH ALL SWITCHES ON.
V- IS CONNECTED TO GND (0V) FOR SINGLE-SUPPLY OPERATION.

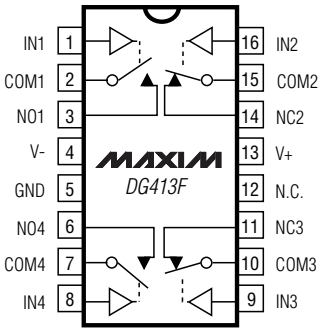
Figure 6. Frequency Response, Off-Isolation, and Crosstalk

Pin Configurations (continued)

TOP VIEW



DIP/TSSOP/SO



DIP/TSSOP/SO

DG412F	
LOGIC	**SWITCH**
0	OFF
1	ON

DG413F		
LOGIC	**SWITCHES 1, 4**	**SWITCHES 2, 3**
0	OFF	ON
1	ON	OFF

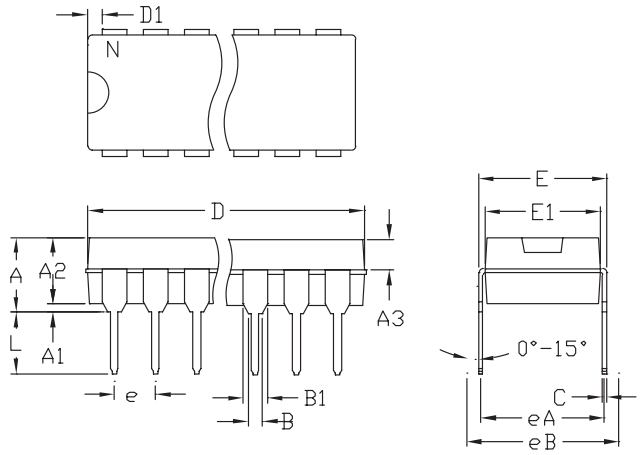
N.C. = NOT CONNECTED. SWITCHES SHOWN FOR LOGIC "0" INPUT.
ALL SWITCHES ARE OFF WITH POWER REMOVED

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.020	---	0.508	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.021	0.381	0.533
B1	0.045	0.060	1.14	1.524
C	0.009	0.014	0.229	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.255
E1	0.275	0.295	6.985	7.493
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	✱5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MS-095-AH
6. N = NUMBER OF PINS

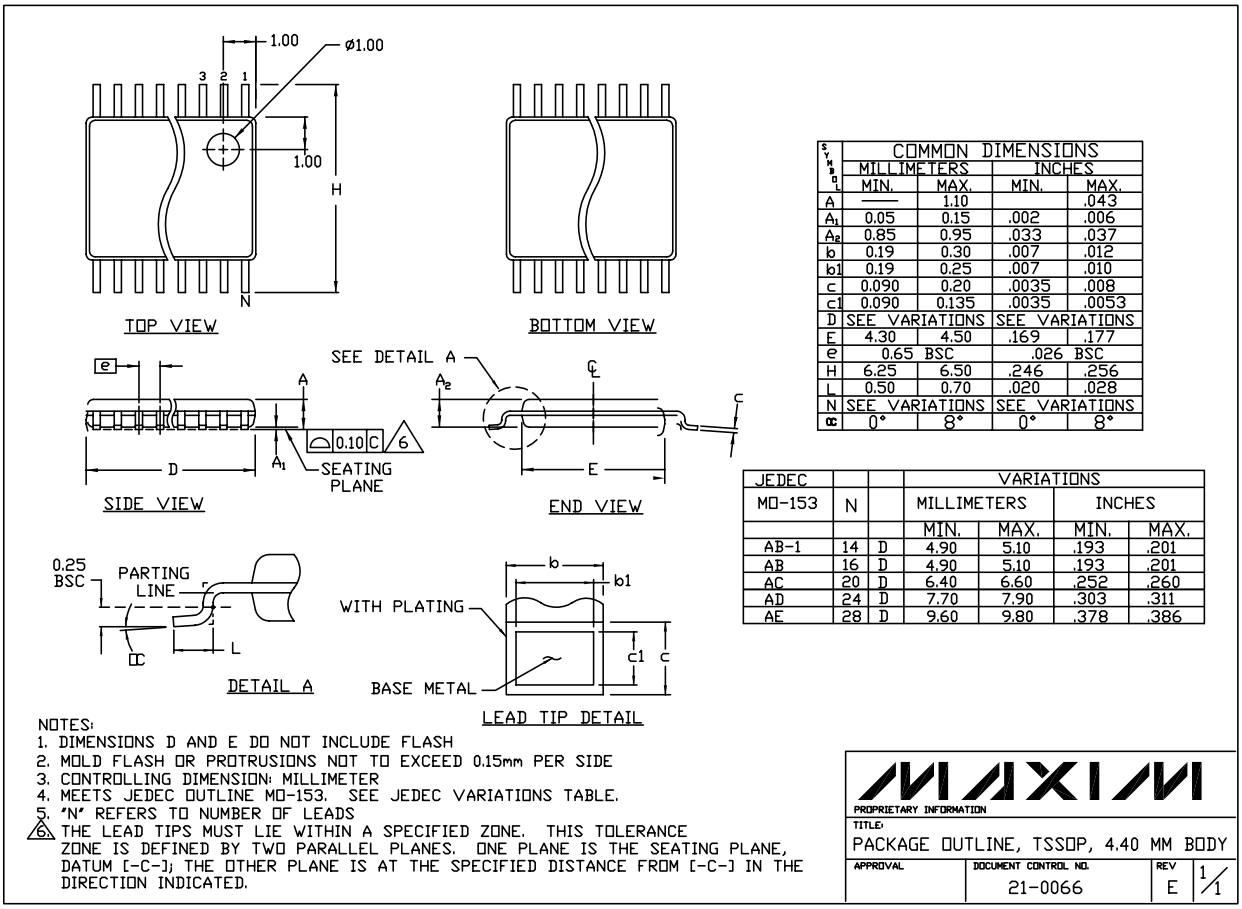
MAXIM — 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" — 1/1 — 21-0043 B (DOCUMENT CONTROL NUMBER — REV)

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

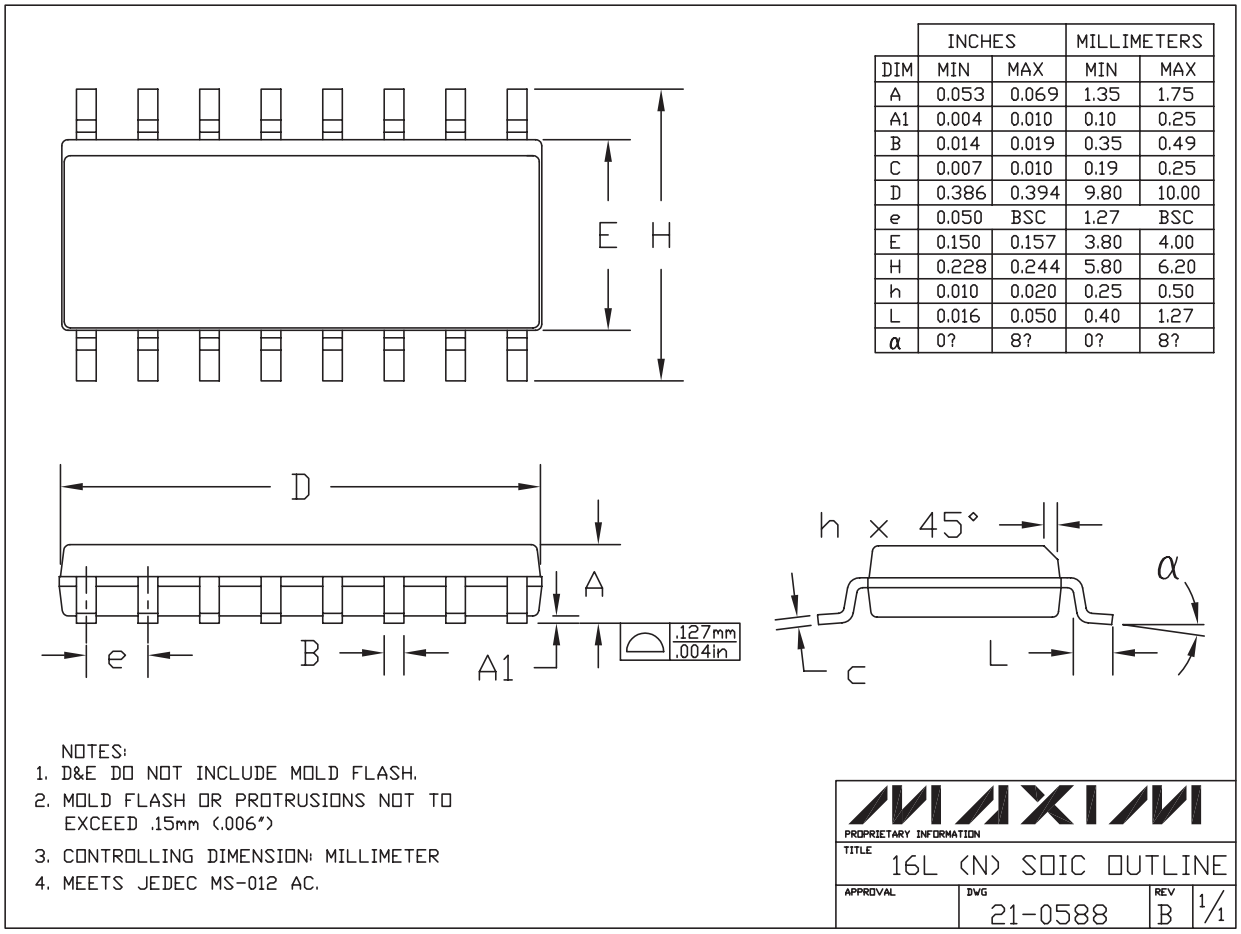
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L SOIC.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0?	8?	0?	8?

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AC.

MAXIM
PROPRIETARY INFORMATION
TITLE: 16L (N) SOIC OUTLINE
APPROVAL | DWG: 21-0588 | REV: B | 1/1

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